Amendments to the Claims

This listing will replace all prior versions, and listing, of claims in the application.

1. (cancelled) A method of forming air gaps between metal leads of a semiconductor device, comprising the steps of:

providing a semiconductor substrate whereby the surface of said semiconductor substrate has been provided with points of electrical contact;

forming a first network of nitride filled trenches in a first level of dielectric said first level of dielectric having been deposited on the surface of said substrate;

forming a second network of nitride filled trenches in a second level of dielectric said second level of dielectric having been deposited on the surface of said first level of dielectric whereby furthermore said second network of nitride filled trenches is in physical contact with and intersects with said first network of nitride filled trenches;

depositing a first thin layer of oxide over the surface of said second layer of dielectric;

etching openings in said first thin layer of oxide said openings to align with said intersects between said first

network of nitride filled trenches and said second network of nitride filled trenches;

removing said nitride from said second network of trenches furthermore removing said nitride from said first network of trenches; and

depositing a second thin layer of oxide over the surface of said first thin layer of oxide thereby closing said openings in said first thin layer of oxide.

2. (cancelled) The method of claim 1 wherein said forming a first network of nitride filled trenches in a first level of dielectric is:

depositing a first layer of dielectric over the surface of said substrate;

patterning and etching said first layer of dielectric thereby creating a first network of trenches in said first layer of dielectric;

depositing a first layer of nitride over the surface of said first layer of dielectric thereby including said first network of trenches; and

polishing said first layer of nitride thereby essentially removing said first layer of nitride from the surface of said first layer of dielectric.

3. (cancelled) The method of claim 1 wherein said forming a second network of nitride filled trenches in a second level of dielectric is:

depositing a second layer of dielectric over the surface of said first layer of dielectric thereby including said first layer of nitride;

patterning and etching said second layer of dielectric thereby creating a second network of trenches in said second layer of dielectric;

depositing a second layer of nitride over the surface of said first layer of dielectric thereby including said second network of trenches; and

polishing said second layer of nitride thereby essentially removing said second layer of nitride from the surface of said second layer of dielectric.

4. (cancelled) The method of claim 1 wherein said first network of trenches intersects said second network of trenches under an angle of about 90 degrees, said angle being measured as an angle

created between a first intersection and a second intersection, said first intersection being an intersection of a first plane of a sidewall of a trench pertaining to said first network of trenches and the surface of said semiconductor substrate, said first plane having been extended towards said surface of said semiconductor substrate to enable intersection therewith, said second intersection being an intersection of a second plane of a sidewall of a trench pertaining to said second network of trenches and the surface of said semiconductor substrate, said second plane having been extended towards said surface of said semiconductor substrate to enable intersection therewith.

5. (cancelled) The method of claim 1 wherein said first network of trenches intersects said second network of trenches under an angle other than 90 degrees, said angle being measured as an angle created between a first intersection and a second intersection, said first intersection being an intersection of a first plane of a sidewall of a trench pertaining to said first network of trenches and the surface of said semiconductor substrate, said first plane having been extended towards said surface of said semiconductor substrate to enable intersection therewith, said second intersection being an intersection of a second plane of a sidewall of a trench pertaining to said second

network of trenches and the surface of said semiconductor substrate, said second plane having been extended towards said surface of said semiconductor substrate to enable intersection therewith.

6. (cancelled) The method of claim 1 with the additional step of further extending the thickness of the combined said first thin layer of oxide and said second layer of oxide thereby enabling the creation of openings of high aspect ratio in the extended layer of oxide combined with said first layer and said second layer of dielectric.

7. (cancelled) The method of claim 6 with the additional step of creating a network of metal interconnect lines on the surface of said extended layer of oxide.

8. (cancelled) The method of claim 1 with the additional step of forming A network of interconnect lines on the surface of said second thin layer of oxide.

9. (cancelled) The method of claim 1 with the additional steps of baking said first level of dielectric and/or said second level of dielectric said baking at a temperature between about 150 and 300 degrees C.

10. (cancelled) The method of claim 1 with the additional steps of curing said first level of dielectric and/or said second level of dielectric at an elevated temperature said curing at a temperature in excess of about 300 degrees C.

11. (cancelled) A method of forming air gaps between metal leads of a semiconductor device, comprising the steps of:

providing a semiconductor substrate whereby the surface of said semiconductor substrate has been provided with points of electrical contact;

forming a first network of trenches in a first level of dielectric said first level of dielectric having been deposited on the surface of said substrate whereby said first network of trenches is filled with a disposable solid layer, creating a first network of disposable solid filled trenches;

forming a second network of trenches in a second level of dielectric said second level of dielectric having been deposited on the surface of said first level of dielectric whereby said

second network of trenches is in physical contact with and intersects with said first network of a disposable solid filled trenches whereby furthermore said second network of trenches is filled with a disposable solid layer, creating a second network of disposable solid filled trenches;

depositing a first thin layer of oxide over the surface of said second layer of dielectric;

etching openings in said first thin layer of oxide said openings to align with said intersects between said first network of trenches and said second network of trenches;

removing said disposable solid layer from said second network of trenches furthermore removing said disposable solid layer from said first network of trenches; and

depositing a second thin layer of oxide over the surface of said first thin layer of oxide thereby closing said openings in said first thin layer of oxide.

12. (cancelled) The method of claim 11 wherein said disposable solid layer is a polymer and whereby said removing said disposable solid layer is exposing said substrate to O_2 oxygen plasma thereby evaporating said disposable solid layer.

13. (cancelled) The method of claim 11 wherein said removing said disposable solid layer is introducing a solvent to said substrate thereby dissolving said disposable solid layer.

14. (cancelled) The method of claim 11 wherein said removing said disposable solid layer is heating said substrate thereby evaporating said disposable solid layer.

15. (cancelled) The method of claim 11 wherein said removing said disposable solid layer is applying a vacuum to said substrate thereby dissolving said disposable solid layer.

16. (cancelled) The method of claim 11 wherein said first network of trenches intersects said second network of trenches under an angle of about 90 degrees, said angle being measured as an angle created between a first intersection and a second intersection, said first intersection being an intersection of a first plane of a sidewall of a trench pertaining to said first network of trenches and the surface of said semiconductor substrate, said first plane having been extended towards said surface of said semiconductor substrate to enable intersection therewith, said second intersection being an intersection of a second plane of a sidewall of a trench pertaining to said second

network of trenches and the surface of said semiconductor substrate, said second plane having been extended towards said surface of said semiconductor substrate to enable intersection therewith.

17. (cancelled) The method of claim 11 wherein said first network of trenches intersects said second network of trenches under an angle other than 90 degrees, said angle being measured as an angle created between a first intersection and a second intersection, said first intersection being an intersection of a first plane of a sidewall of a trench pertaining to said first network of trenches and the surface of said semiconductor substrate, said first plane having been extended towards said surface of said semiconductor substrate to enable intersection therewith, said second intersection being an intersection of a second plane of a sidewall of a trench pertaining to said second network of trenches and the surface of said semiconductor substrate, said second plane having been extended towards said surface of said semiconductor substrate to enable intersection therewith.

18. (cancelled) The method of claim 11 with the additional

step of further extending the thickness of the combined said first thin layer of oxide and said second layer of oxide thereby enabling the creation of openings of high aspect ratio in the extended layer of oxide combined with said first layer and said second layer of dielectric.

19. (cancelled) The method of claim 18 with the additional step of creating a network of metal interconnect lines on the surface of said extended layer of oxide.

20. (cancelled) The method of claim 11 with the additional step of forming a network of interconnect lines on the surface of said second thin layer of oxide.

21. (cancelled) The method of claim 11 with the additional step of baking said first level of dielectric and/or said second level of dielectric said baking at a temperature between about 150 and 300 degrees C.

22. (cancelled) The method of claim 11 with the additional step of curing said first level of dielectric and/or said second level of dielectric at an elevated temperature said curing at a temperature in excess of about 300 degrees C.

23. (cancelled) A method of forming air gaps between metal leads of a semiconductor device, comprising the steps of:

providing a semiconductor substrate;

depositing a layer of metal on the surface of said substrate;

etching said metal layer in a pattern to form metal leads, said metal leads running in a Y-direction said metal leads furthermore having top surfaces;

depositing a first layer of dielectric over the surface of said substrate thereby including said metal leads;

creating trenches in said first level of dielectric said trenches running in a X-direction;

filling said trenches in said first layer of dielectric with a first layer of nitride or another disposable solid;

depositing a second layer of dielectric over the surface of said first layer of dielectric thereby including said first layer of nitride or another disposable solid;

creating trenches in said second level of dielectric said trenches running in a Y-direction said trenches furthermore having intersects with said trenches created in said first layer of dielectric;

filling said trenches in said second layer of dielectric with a second layer of nitride or another disposable solid;

depositing a first thin layer of oxide over the surface of said second layer of dielectric thereby including the surface of said second layer of nitride or other disposable solid;

etching openings in said first thin layer of oxide said openings to align with said intersects between said trenches created in said first level of dielectric and said trenches created in said second layer of dielectric;

removing said second layer of nitride or other disposable solid from said trenches created in said second layer of dielectric furthermore removing said first layer of nitride or other disposable solid from said trenches created in said first layer of dielectric thereby creating a network of trenches in said first layer of dielectric and in said second layer of dielectric whereby said trenches in said first layer of dielectric intersect said trenches in said second layer of dielectric under an angle of about 90 degrees, said angle of about 90 degrees being measured as an angle created between a first intersection and a second intersection, said first intersection being an intersection of a first plane of a sidewall of a trench pertaining to said trenches created in said first level of dielectric and the surface of said semiconductor substrate, said first plane having been extended towards said surface of said semiconductor substrate to enable intersection

therewith, said second intersection being an intersection of a second plane of a sidewall of a trench pertaining to said trenches created in said second layer of dielectric and the surface of said semiconductor substrate, said second plane having been extended towards said surface of said semiconductor substrate to enable intersection therewith; and

depositing a second thin layer of oxide over the surface of said first thin layer of oxide thereby closing off said openings in said first thin layer of oxide.

24. (cancelled) The method of claim 23 wherein said whereby said trenches in said first layer of dielectric intersect said trenches in said second layer of dielectric under an angle other than 90 degrees, said angle of about 90 degrees being measured as an angle created between a first intersection and a second intersection, said first intersection being an intersection of a first plane of a sidewall of a trench pertaining to said trenches created in said first level of dielectric and the surface of said semiconductor substrate, said first plane having been extended towards said surface of said semiconductor substrate to enable intersection therewith, said second intersection being an intersection of a second plane of a sidewall of a trench pertaining to said trenches created in said

second layer of dielectric and the surface of said semiconductor substrate, said second plane having been extended towards said surface of said semiconductor substrate to enable intersection therewith.

25. (currently amended) A multilevel interconnect structure, comprising:

a semiconductor surface that has been provided with points of electrical contact in ~~the surface of~~ said surface;

a first layer of dielectric deposited on said semiconductor surface, said first layer of dielectric containing a first network of trenches filled with air;

a second layer of dielectric deposited on said semiconductor surface, said second layer of dielectric containing a second network of trenches filled with air, whereby said second network of trenches is in physical contact with and intersects with said first network of trenches under an angle ~~of known value~~; and

a layer of oxide deposited over ~~the surface of~~ said second layer of dielectric.

26. (currently amended) The multilevel interconnect structure of claim 25 whereby furthermore a network of metal interconnect lines is created on ~~the surface of~~ said layer of oxide.

27. (currently amended) The multilevel interconnect structure of claim 25 whereby furthermore said layer of oxide deposited over ~~the surface of~~ said second layer of dielectric trenches is extended in thickness ~~by a measurable amount~~.

28. (currently amended) The multilevel interconnect structure of claim 27 whereby furthermore a network of metal interconnect lines is created on ~~the surface of~~ said extended layer of oxide.